02-27-03

Gp/2815

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Docket Number: 10746/23

Application Number	Filing Date	Examiner	Art Unit
09/754,632	January 4, 2001	Not Yet Assigned	2815

Title: FUNCTION RECONFIGURABLE SEMICONDUCTOR DEVICE AND INTEGRATED CIRCUIT CONFIGURING THE SEMICONDUCTOR DEVICE

Applicant(s): Kazuo Aoyama et al.

Address to:
Commissioner for Patents
Washington, D.C. 20231

1. In accordance with the duty of disclosure under 37 C.F.R. § 1.56 and in conformance with the procedures of 37 C.F.R. §§ 1.97 and 1.98 and M.P.E.P. § 609, attorney(s) for Applicant(s) hereby bring the reference(s) listed on the attached modified PTO Form No. 1449 to the attention of the Examiner. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

2. A copy of each patent, publication or other information listed on the modified PTO form 1449 is enclosed, except as otherwise indicated.

3. Pursuant to 37 C.F.R. § 1.97(c) and § 1.97(e), Applicants' attorney certifies that each item of information contained in the information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign (European) patent application not more than three months prior to the filing of information disclosure statement.

4. While no fee is believed to be due, the Commissioner is authorized (as appropriate or necessary) to charge any fees or credit any overpayment to Deposit Account No. **11-0600**. A duplicate copy of this transmittal letter is enclosed for that purpose.

Dated: 2/25/2003 By: _____

Aaron C. Deditch (Reg. No. 33,865)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT PTO-1449 FORM	ATTY. DOCKET NO. 10746/23	U.S. SERIAL NO. 09/754,632
	APPLICANT(S) Aoyama, et al.	
	FILING DATE January 4, 2001	GROUP 2815

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	PATENT NUMBER	PATENT DATE	NAME	CLASS	SUBCLASS	FILING DATE*
	5 990 709	November 23, 1999	Thewes, et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	0 566 739	October 27, 1993	Europe				
	0 685 807	December 6, 1995	Europe				

OTHER DOCUMENTS

EXAMINER INITIAL		AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
		Kotani, K., et al. "Neuron-MOS binary-logic circuits featuring dramatic reduction in transistor count and interconnections" ELECTRON DEVICES MEETING, 1992. TECHNICAL DIGEST., INTERNATIONAL SAN FRANCISCO, CA, USA 13-16 DEC. 1992, NEW YORK, NY, USA, IEEE, US, 13 December 1992, pp. 431-434.
		Tadashi, Shibata, et al. "Neuron MOS Voltage-Mode Circuit Technology for Multiple-Valued Logic" IEICE Transactions on Electronics, Institute of Electronics Information and Comm. Eng. Tokyo, JP, vol. E76-C, no.3, 1 March 1993, pp. 347-356.

EXAMINER	DATE CONSIDERED
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

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